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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,350	03/02/2004	Michael W. Leddige	5038-356	4528

32231 7590 11/20/2006

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EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,350	LEDDIGE ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/2/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *9-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-8, drawn to a memory module and system including: first and second outer columns that can be interchanged, and not including: a module to receive the memory array and arranging the fixed set of memory signals in inner columns of a connection array.

II. Claims 9-11, drawn to a memory device including: a module to receive the memory array, and not including: first and second outer columns that can be interchanged and arranging the fixed set of memory signals in inner columns of a connection array.

III. Claims 12-16, drawn to a method for designing a memory device including: arranging the fixed set of memory signals inner columns of a connection array, and not including: first and second outer columns that can be interchanged and a module to receive the memory array.

2. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Julie L. Reed on 8/28/2006, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-8. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 9-16 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-8 are rejected under 35 U.S.C. 102(e)** as being anticipated by Dickmann (US PG Pub 2004/0230932).

6. With respect to claims 1 and 5, Dickmann teaches:

a first memory module mounted on a first side of a substrate (memory modules that comprise chips IC1-IC36 are plugged into a motherboard [substrate] – a printed circuit board acting as a first layer, paragraph [0034]), the first memory module comprising:

an array of connections arranged in rows and columns (see Fig 3, rows and columns of memory chip array; also see "row arrangements", paragraph [0036]) such that there are first and second outer columns (M1 and M4 out columns of Figure 3, also see "the two outer modules", M1 and M4, paragraph [0036]), and that connections in the first and second outer columns can be interchanged (i.e. data interchange is performed between the semiconductor chips in the selected group [i.e. outer columns

M1 and M4 –see paragraph 0020 with respect to selection probability], paragraph [0014]);

a second memory module mounted on a second side of the substrate (chips distributed over both sides, paragraph [0038]), comprising:

an array of connections arranged in rows and columns (see Fig 3, rows and columns of memory chip array; also see "row arrangements", paragraph [0036]) such that there are first and second outer columns (M1 and M4 out columns of Figure 3, also see "the two outer modules", M1 and M4, paragraph [0036]), and that connections in the first and second outer columns can be interchanged (i.e. data interchange is performed between the semiconductor chips in the selected group [i.e. outer columns M1 and M4 –see paragraph 0020 with respect to selection probability], paragraph [0014]);

a memory controller to control interchange of signals between first and second outer columns of the memory modules (i.e. memory controller whose job is to control the data interchange between the processor and the memory, paragraph [0006]);

signal traces in the substrate (see interconnections of Fig 3), wherein the connection in the first and second outer columns of the first and second memory modules are arranged such that signals routed on the traces have uniform routing lengths (Fig 3 suggests routing lengths are uniform).

7. With respect to claim 2, Dickmann teaches all the elements of claim 1, from which the claim depends. Dickmann teaches: wherein the first outer column is a nearside column (see Fig 3, outer column M4 is nearest to memory controller C) and

the second outer column is far-side column (see Fig 3, outer column M1 is farthest from the memory controller C).

8. With respect to claim 3, Dickmann teaches all the elements of claim 1, from which the claim depends. Dickmann teaches: wherein there are third and fourth outer columns having interchangeable connections (i.e. interchange is performed between the semiconductor chips in the selected group, wherein paragraphs [0018-0020] suggest that the selected group comprise the modules [i.e. columns]) M1 and M4, or M2 and M3, or another combination, see paragraphs [0014], [0018], and [0020]).

9. With respect to claims 4 and 8, Dickmann teaches all the elements of claims 1 and 5, from which the claims depend respectively. Dickmann teaches: the memory module further comprising a package selected from the group comprised of: X16, and X4/X8 (x4, see paragraph [0041]).

10. With respect to claim 6, Dickmann teaches all the elements of claim 5, from which the claim depends. Dickmann teaches: the substrate further comprising a multi-layered printed circuit board (i.e. memory modules plugged into a motherboard, paragraph [0034]).

11. With respect to claim 7, Dickmann teaches all the elements of claim 6, from which the claim depends. Dickmann teaches: signal traces further comprising multiple signal traces in multiple layers of the printed circuit board (i.e. discussion of the arrangement in a printed circuit board, paragraph [0036]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

PAUL DINH
PRIMARY EXAMINER